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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/059,644	04/13/98	PAN P	MI22-898

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EXAMINER	
TRINH, M	
ART UNIT	**PAPER NUMBER**
2822	5

DATE MAILED: 09/16/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/059,644	Pan
Examiner	**Group Art Unit**
Michael Trinh	2822

☒ Responsive to communication(s) filed on *Apr 13, 1998*.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *41-52* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *41-52* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *4*

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

Part III DETAILED ACTION

*** Preliminary amendment filed April 13, 98 has been entered as paper number 2/A. Claims 1-40 were canceled. Claims 41-52 have been newly added.

Claim Rejections - 35 USC § 112

1. Claims 43,45-49,52 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 52, line 3, "substrate dielectric surface" is unclear and indefinite since it is a surface of what layer and formed on where. As disclosed, the phrase is understood and meant as --a surface of a dielectric layer formed on a semiconductor substrate--.

In claim 52, line 3, the term "patterned" is non-sequitur since no patterning step has been previously recited in claim 52.

In claim 52, line 16, "the oxidation barriers on the gate" is unclear and lacking proper antecedent basis. It should be --oxidation barrier spacers on sidewalls of the gate--.

In claim 43, line 4, "the overlying layer" lacks proper antecedent basis, and should be --the overlying metal--.

In claim 45, "...over a substrate gate's sidewalls...all conductive material" and "...through a layer which underlies the gate...and which is outwardly exposed..." are non-sequitur and unclear, since no previous steps in claim 45 have been expressly recited to form a gate having sidewalls and the layer so that sidewall spacers can be formed. Moreover, it is unclear the gate and the layer are formed on where.

In claim 45: last step is incomplete and indefinite for what is oxidized, and should be --...oxidizing at least a portion of the gate...--.

2. Claims 41,43-49 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. Claim 41, line 6, and Claim 45, line 3, simply recite "forming sidewall spacers over...". However, specification required to form sidewall spacers of an oxidation resistant material. Thus, --forming oxidation resistant sidewall spacers-- is critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure to form a smiling gate as disclosed. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

(Dependent claims are rejected as depending on rejected base claim)

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321© may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 41-52 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-41 of U.S. Patent No. 5,739,066. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims are drawn to the same invention for oxidizing a portion of the gate interface with the gate dielectric layer, and broad enough to encompass the scope of claims 1-41.

Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the parent application which is now US Patent 5,739,066. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention there of by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent

6. Claims 45,46,49 are rejected under 35 U.S.C. § 102(e) as being anticipated by Park et al (5,545,578).

Park et al teach a method for forming a conductive gate of a metal oxide transistor comprising the steps of: forming sidewall spacers 22a (fig 4E) to cover sidewalls of a conductive gate 16a; and then conducting an oxidizing step by channeling oxidants through a layer 12 and 14a underlying the gate and the sidewall spacers 22a, and which is outwardly exposed laterally proximate the sidewall spacers, wherein forming the spacers includes anisotropically etching a first material 22 to form first spacers, depositing a second material, and anisotropically etching to the second material to form second spacers 28 (fig 4H; col 4, line 25 through col 5).

7. Claims 41,45,46 are rejected under 35 U.S.C. § 102(b) as being anticipated by Chen (4,786,609).

Chen teaches a method for forming a conductive gate of a metal oxide transistor comprising the steps of: forming a gate structure having a polysilicon gate formed on a gate oxide dielectric layer 9 formed on a semiconductor substrate; forming sidewall spacers 34 over sidewalls of the gate and joining the dielectric oxide layer left intact (fig 2F; col 4, line 53 through col 5; col 4, lines 9-42); and oxidizing the substrate to channel oxidants through the gate dielectric layer and underneath the spacers to oxidize at least a portion of the gate including a portion interfacing with the gate dielectric layer (fig 1g; col 5, line 3+), and which is outwardly exposed laterally proximate the sidewall spacers.

8. Claims 41-42,45-46,50 are rejected under 35 U.S.C. § 102(b) as being anticipated by Koyama (JP 64 73772).

Koyama teaches a method for forming a conductive gate of a metal oxide transistor comprising the steps of: forming a gate structure having a polysilicon gate 4 formed on a gate oxide dielectric layer 3 formed on a semiconductor substrate (figs 1a,3a,4a; Abstract); forming sidewall nitride spacers 12a over sidewalls of the gate and joining the dielectric oxide layer (figs 1c,3c,,4c) by anisotropically etching a silicon nitride layer 12 (figs 1-4); and oxidizing the substrate to channel oxidants through the gate dielectric layer 3 and underneath the spacers to oxidize at least a portion of the gate including a portion interfacing with the gate dielectric layer (as shown in figs 1d,3d,4d,5b), and which is outwardly exposed laterally proximate the sidewall spacers, wherein oxidizing a portion of the gate would form the oxide layer 11 as shown in figure 1d,3d,4d thicker than the oxide layer 11 as shown in figures 1c,3c,4c.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 41-43,45-47,50 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Koyama (JP 64 73772) and/or Park et al (5,545,578) and/or Chen (4,786,609), taken with Pintchovski et al (5,126,283).

Koyama and/or Park et al and/or Chen teach a method for forming a conductive gate of a metal oxide transistor as applied above, but lack to form a gate having a polysilicon, a conductive reaction barrier layer, and an overlying metal (re claims 43,47).

However, Pintchovski et al teach (at figs 3a-3c; col 5, line 60 through col 6, line 45) to alternatively form a gate having a polysilicon layer 38, a conductive reaction barrier layer 40, and an overlying metal 42.

The subject matter would have been obvious to one of ordinary skill in the art at the time the invention was made to form a multi-layered transistor gate as taught by Pintchovski et al because of the desirability to fabricate high speed devices.

11. Claims 44,48,49,51,52 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Koyama (JP 64 73772) and/or Park et al (5,545,578) and/or Chen (4,786,609), taken with Pintchovski et al (5,126,283), as applied to claims 41-43,45-47,50 above, and further of Brigham et al (5,714,413) and Kumagai et al (5,430,313).

As previously applied, the relied references teach to form single sidewall barrier spacers on sidewalls of the gate, which teaching is directed to a first embodiment of the present invention as shown in figure 3, in which single sidewall barrier spacers 34 are used.

The further main difference between the references applied above and the instant claim(s) is as follows: the present application, in a second embodiment (fig 5) and in a third embodiment

(fig 7), instead of using single sidewall spacers as in the first embodiment (fig 3), forming and using double sidewall spacers by etching first and second material layers.

However, Brigham et al teach (at figs 2b-2c,3c; col 6, line 60 through col 7, line 6; cols 4-6) to form double sidewall spacers by depositing a second material layer on a first material layer and anisotropically etching the first and second layers to form double sidewall spacers, wherein Brigham expressly teaches "three or more layers of dielectric...are implemented to form a multi-layered spacer structures" (col 6, lines 1-6), and wherein silicon nitride is disclosed. Kumagai et al teach (at figs 4B-4D; col 3, line 65 through col 4, line 15) to form single sidewall nitride spacers 16 on sidewalls of a gate 14, and alternatively, forming double sidewall nitride spacers including first sidewall nitride spacers 16 and second sidewall nitride spacers 30 by anisotropically etching a deposited first material barrier layer and then anisotropically etching a second deposited material barrier layer (figs 7A-7D; col 5, line 45 through col 6).

The subject matter would have been obvious to one of ordinary skill in the art at the time the invention was made to alternatively form single sidewall nitride spacers or double sidewall spacers on the sidewalls of the gate as combinatively taught by Brigham, Kumagai, Koyama, Park et al. This is because of the desirability to substitute and to alternatively use the single sidewall nitride spacers or the double sidewall spacers as a barrier mask during oxidation to form an oxide film, and also because of the desirability to employ the double sidewall spacers as a mask during implantation to form source and drain regions.

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*** This office action has been created under the Patent and Trademark Office Semiconductor Technology Quality Assurance Pilot Program. It incorporates the examination quality standards set as a result of customer focus sessions with the semiconductor industry. The listing of the field of search to follow is one of these standards.

Field of Search	Date
U.S. Class and subclass: 438/595,305,306,307,303,770	9/8/99

*** Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Trinh whose telephone number is (703) 308-2554. The examiner can normally be reached on Monday through Friday, from 8:30 Am to 5:00 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Whitehead Jr, Carl, can be reached on (703) 308-4940. The fax phone number for this Group is (703) 305-3432 or (703) 308-7382.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-1782.

-d31-

Michael Trinh
Primary Examiner